VLSI SYSTEM DESIGN (121146)

1) Also affiliated with SiTel Semiconductor, Design Center Hengelo.

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GOALS

• Familiarity with modern VLSI design techniques with an emphasis on system-level design issues.
• Knowledge of design flow and design automation tools used.
• Reaching a level beyond basic VHDL simulation and synthesis.

SHORT CONTENTS (TENTATIVE)

• Low-power design at register-transfer and system levels.
• Asynchronous design
• Advanced verification:
  – Formal verification
  – Testbench design, transaction-level modeling, etc.
  – SystemC
• Advanced VLSI architectures: e.g. networks-on-chip (NoCs)

REQUIRED KNOWLEDGE

• In principle, this course is a follow-up to the System-on-Chip Design course, especially the part HDL-Based Design. Those that have finished this part are automatically admitted.
• Older generation students who have finished the ASIC Design Laboratory are also automatically admitted.
• Students with another preparation can be admitted after approval by the instructor (Sabih Gerez).
COURSE MATERIAL

- **No book**, but a **collection of papers**. To be announced on the course’s web page with URL:
  

- **Lecture slides**. To become available through the web page.

LECTURES

- 6 or 7 lectures on Mondays 3rd/4th hour;
- According to official schedule; beware of holidays and examination periods!

**STUDY LOAD: 140 hours**

- Max. 40 hours for attending lectures and studying paper material.
- Some 100 hours left for project work.

EXAMINATION

- Practical project. Exact form not yet known. Any (combination of):
  - Relatively small exercises.
  - Large design project.
  - Design contest.
  - Literature study.
- Individually or in teams of two students.
- Oral examination on theory in combination with project discussion determines final mark.

RELATED COURSES

- VLSI Signal Processing (121095)
- CAD Tools for VLSI (121097)
- Digital VLSI Circuit Design (121133)
- Testable Design and Test of Nanosystems (121132)
- Hardware/Software Co-Design (213012)