Topics

- Block placement.
- Channel and switchbox routing.
- Global routing.
- Power/ground routing.
- Clock routing.
- Floorplanning tips.
- Off-chip connections.

Floorplanning strategies

- Floorplanning must take into account blocks of varying function, size, shape.
- Must design:
  - space allocation;
  - signal routing;
  - power supply routing;
  - clock distribution.

Floorplanning strategies

Bricks-and-mortar floorplan

blocks

standard cell

RAM

data path

Purposes of floorplanning

- Early in design:
  - Prepare a floorplan to budget area, wire area/delay. Tradeoffs between blocks can be negotiated.
- Late in design:
  - Make sure the pieces fit together as planned.
  - Implement the global layout.
Types of routing

- Channel routing:
  - channel may grow in one dimension to accommodate wires;
  - pins generally on only two sides.
- Switchbox routing:
  - cannot grow in any dimension;
  - pins are on all four sides, fixing dimensions of the box.

Channels and switchboxes

[Diagrams of Channel and Switchbox routing]

Block placement

- Blocks have:
  - area;
  - aspect ratio.
- Blocks may be placed at different rotations and reflections.
- Uniform size blocks are easier to interchange.

Blocks and wiring

- Cannot ignore wiring during block placement—large wiring areas may force rearrangement of blocks.
- Wiring plan must consider area and delay of critical signals.
- Blocks divide wiring area into routing channels.
Channel definition

- Channels end at block boundaries.
- Several alternate channel definitions are possible:

Channels must be routed in order

Wire out of end of one channel creates pin on side of next channel:

Slicable floorplan

Channel Order in a Slicable Floorplan
Windmills or Wheel Floorplans

- The floorplan is not slicing;
- No channel ordering exists;
- Switchbox routing next to channel routing is required.

Global routing

- Goal: assign wires to paths through channels.
- Don’t worry about exact routing of wires within channel.
- Can estimate channel height from global routing.

Channel utilization

- Want to keep all channels about equally full to minimize wasted area.
- Important to route time-critical signals first.
- Shortest path may not be best for global wiring.
- In general, may need to rip-up wires and reroute to improve the global routing.

Power distribution

- Must size wires to be able to handle current—requires designing topology of V_{DD}/V_{SS} networks.
- Want to keep power network in metal—requires designing planar wiring.
Interdigitated power and ground lines

VDD

VSS

Power supply noise

- Variations in power supply voltage manifest themselves as noise into the logic gates.
- Power supply wiring resistance creates voltage variations with current surges.
- Voltage drops on power lines depend on dynamic behavior of circuit.

Tackling power supply noise

- Must measure current required by each block at varying times.
- May need to redesign power/ground network to reduce resistance at high current loads.
- Worst case, may have to move some activity to another clock cycle to reduce peak current.

Clock distribution

- Goals:
  - deliver clock to all memory elements with acceptable skew;
  - deliver clock edges with acceptable sharpness.
- Clocking network design is one of the greatest challenges in the design of a large chip.
Clocks are generally distributed via wiring trees.

- Want to use low-resistance interconnect to minimize delay.
- Use multiple drivers to distribute driver requirements—use optimal sizing principles to design buffers.
- Clock lines can create significant crosstalk.

Clock distribution tree example: DEC Alpha 21164

- See figure on page 380.
- Pre-clock drivers at the center of the chip.
- Two clock-driver blocks at the left and right with 44 drivers each.
- The last level: regular grid across entire chip.
- Uses metal layer 3 and 4.
- Total load: 3.75 pF.

Floorplanning tips

- Develop a wiring plan. Think about how layers will be used to distribute important wires.
- Sweep small components into larger blocks. A floorplan with a single NAND gate in the middle will be hard to work with.
- Design wiring that looks simple. If it looks complicated, it is complicated.
Floorplanning tips, cont’d.

- Design planar wiring. Planarity is the essence of simplicity. It isn’t always possible, but do it where feasible (and where it doesn’t introduce unacceptable delay).
- Draw separate wiring plans for power and clocking. These are important design tasks which should be tackled early.

Off-chip connections

- A package holds the chip. Packages can introduce significant inductance.
- Pads on the chip allow the wires on chip to be connected to the package. Pads are library components which require careful electrical design.

Structure of a typical package

- Pads are placed on top-layer metal to provide a place to bond to the package.
- Pads are typically placed around periphery of chip.
- Some advanced packaging systems bond directly to package without bonding wire; some allow pads across entire chip surface.

I/O architecture
Pad frame architecture

Pad frame design
- Must supply power/ground to each pad as well as chip core.
- Positions of pads around frame may be determined by pinout requirements on package.
- Want to distribute power/ground pins as evenly as possible to minimize power distribution problems.

Input pads
- Main purpose is to provide electrostatic discharge (ESD) protection.
- Gate voltage of transistor is very sensitive—can be permanently damaged by high voltage.
- Static electricity in room is sufficient to damage CMOS ICs.

Output pad circuits
- Don’t need ESD protection—transistor gates not connected to pad.
- Must be able to drive capacitive load of pad + outside world.
- May need voltage level shifting, etc. to be compatible with other logic families.
Three-state pad

- Combination input/output, controlled by mode input on chip.
- Pad includes logic to disconnect output driver when pad is used as input.
- Must be protected against ESD.

Three-state pad circuit

Boundary scan

- Boundary scan is a technique for testing chips on boards. Pads on chips are arranged into a scan chain that can be used to observe and control pins of all chips.
- Requires some control circuitry on pads along with an on-chip controller and boundary-scan-mode control pins.