Topics

- Memories:
  - ROM;
  - SRAM;
  - DRAM.
- PLAs.

High-density memory architecture

Memory operation

- Address is divided into row, column.
  - Row may contain full word or more than one word.
- Selected row drives/senses bit lines in columns.
- Amplifiers/drivers read/write bit lines.

Read-only memory (ROM)

- ROM core is organized as NOR gates—pull-down transistors of NOR determine programming.
- Erasable ROMs require special processing that is not typically available.
- ROMs on digital ICs are generally mask-programmed—placement of pull-downs determines ROM contents.
ROM core circuit

Static RAM (SRAM)

- Core cell uses six-transistor circuit to store value.
- Value is stored symmetrically—both true and complement are stored on cross-coupled transistors.
- SRAM retains value as long as power is applied to circuit.

SRAM core cell

SRAM core operation

- **Read:**
  - precharge bit and bit’ high;
  - set select line high from row decoder;
  - one bit line will be pulled down.
- **Write:**
  - set bit/bit’ to desired (complementary) values;
  - set select line high;
  - drive on bit lines will flip state if necessary.
SRAM sense amp

![SRAM Sense Amp Diagram]

**Sense amp operation**

- Differential pair—takes advantage of complementarity of bit lines.
- When one bit line goes low, that arm of diff pair reduces its current, causing compensating increase in current in other arm.
- Sense amp can be cross-coupled to increase speed.

3-transistor dynamic RAM (DRAM)

- First form of DRAM—modern commercial DRAMs use one-transistor cell.
- 3-transistor cell can easily be made with a digital process.
- Dynamic RAM loses value due to charge leakage—must be refreshed.

3-T DRAM core cell

![3-T DRAM Core Cell Diagram]
3-T DRAM operation

- Value is stored on gate capacitance of $t_1$.
- **Read:**
  - read = 1, write = 0, read_data’ is precharged;
  - $t_1$ will pull down read_data’ if 1 is stored.
- **Write:**
  - read = 0, write = 1, write_data = value;
  - guard transistor writes value onto gate capacitance.

One-Transistor DRAM

- Capacitor is not parasitic but intentional.
- Read operation (precharge bit line) is destructive; refresh is necessary.
- Special requirements for sense amplifiers.

Flash Memory

- Non-volatile memory (not erased when power is off).
- By applying high voltages on the “regular gate”, charge gets trapped on floating gate.

Programmable logic array (PLA)

- Used to implement specialized logic functions.
- A direct implementation of the *sum-of-products* form.
- A PLA decodes only some addresses (input values); a ROM decodes all addresses.
- PLA not as common in CMOS as in nMOS, but is used for some logic functions.
**PLA organization**

- AND plane
- OR plane
- p1, p2, p3, p4
- f0, f1
- i0, i0', i1, i1'
- product term

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**PLA structure**

- AND plane, OR plane, inverters together form complete two-level logic functions.
- Both AND and OR planes are implemented as NOR circuits.
- Pull-down transistors form programming/personality of PLA. Transistors may be referred to as programming tabs.

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**Precharged bus circuit (PLA NOR gate)**

- Diagram showing the precharged bus circuit with inputs and outputs.