Topics

- Design methodologies.
- Kitchen timer example (not covered in lecture; check by yourself).

Design methodologies

- Every company has its own design methodology.
- Methodology depends on:
  - size of chip;
  - design time constraints;
  - cost/performance;
  - available tools.

Generic design flow

- Specification and planning

  - Driven by contradictory impulses:
    - customer-centric concerns about cost, performance, etc.;
    - forecasts of feasibility of cost and performance.
  - Features, performance, power, etc. may be negotiated at early stages; negotiation at later stages creates problems.
Estimation and planning

- Estimation techniques vary with module:
  - memories may be generated once size is known;
  - data paths may be estimated from previous design;
  - controllers are hard to estimate without details.
- Estimates must include speed, area, power.

Floorplanning and budgeting

- The purpose of early floorplanning is to establish budgets for each major component: area, delay, power, etc.
- The project leader must ensure that budgets are met at all times. If it becomes clear that meeting a budget for a component is impossible, the floorplan must be redone ASAP.

Logic design

- For controllers, good state assignment is usually requires CAD tools.
- Logic synthesis is an option:
  - very good for non-critical logic;
  - can work well for speed-critical logic.
- Logic synthesis system may be sensitive to changes in the input specification.

Circuit/layout design

- Tasks:
  - size transistors;
  - draw layout.
- Alternative design styles:
  - full custom logic (very tedious);
  - standard cell.
- Full custom most likely for datapaths, least likely for random logic off critical path.
Design validation

- Must verify:
  - layout (design rule check = DRC);
  - circuit performance;
  - clock distribution;
  - functionality;
  - power consumption / power bussing.

Testing

- Automatic test pattern generation = ATPG.
- Must verify that circuit can be tested, generate a compact set of manufacturing test vectors.
- Test vectors often comprised of vectors taken from simulation + ATPG-generated vectors.

Tapeout

- Tapeout: generating final files for masks. Shipped to mask-making house.
- Pre-tapeout verification is importance since it will take months to get results from fab.
- Tapeout party follows. Size of party depends on importance of chip design project.