**Topics**

- Basic fabrication steps
- Transistor structures
- Basic transistor behavior
- Parasitics

**Fabrication services**

- Educational services:
  - U.S.: MOSIS
  - EU: EuroPractice
  - Taiwan: CIC
  - Japan: VDEC
- Foundry = fabrication line for hire.

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**Fabrication processes**

- IC built on top of silicon *substrate* (partially diffused into it)
- Substrate regions are doped with *n-type* and *p-type* impurities (with *electron* and *hole* mobility respectively).
- Wires made of polycrystalline silicon (poly), multiple layers of aluminum (metal).
- Silicon dioxide (SiO$_2$) is insulator.

**Photolithography**

- Mask patterns are put on wafer using photosensitive material:
Process steps

First place tubs to provide properly-doped substrate for n-type, p-type transistors:

- **p-tub**
- **n-tub**
- **substrate**

Process steps, cont’d.

Pattern polysilicon before diffusion regions:

- **poly**
- **gate oxide**
- **poly**

Process steps, cont’d

Add diffusions, performing self-masking:

- **n+**
- **p-tub**
- **n+**
- **p+**
- **n-tub**
- **p+**

- **n-type transistor**
- **p-type transistor**

Process steps, cont’d

Start adding metal layers:

- **metal 1**
- **vias**
Transistor structure

n-type transistor:

- SiO₂
- source (n+)
- channel
- drain (n+)
- substrate (p)

0.25 micron transistor (Bell Labs)

- gate oxide
- silicide
- source/drain
- poly

Transistor layout

- “W over L” ratio is an important characteristic.
- The wider the transistor, the more current it can carry, the faster it can switch.
- p-type transistors have less conductivity (holes have a lower mobility than electrons) and are often wider.

Gate voltage and the channel

- $ds < V_{gs} - V_t$
- $ds = V_{gs} - V_t$
- $ds > V_{gs} - V_t$
Drain current characteristics

\[ V_{GS} = 6V \]
\[ V_{GS} = 2.5V \]
\[ V_{GS} = 1.5V \]

Transistor gate parasitics

- Gate-source/drain overlap capacitance:
- Gate capacitance \( C_g \): Determined by active area.
- Source/drain overlap capacitances \( C_{gs}, C_{gd} \): Determined by source/gate and drain/gate overlaps. Independent of transistor L.
  - \( C_{gs} = C_{ol} W \)
- Gate/bulk overlap capacitance.

Wires and vias
Metal migration

- Current-carrying capacity of metal wire depends on cross-section. Height is fixed, so width determines current limit.
- Metal migration: when current is too high, electron flow pushes around metal grains. Higher resistance increases metal migration, leading to destruction of wire.

Metal migration: problems and solutions

- Marginal wires will fail after a small operating period—*infant mortality*.
- Normal wires must be sized to accommodate maximum current flow: $I_{\text{max}} = 1.5 \text{ mA}/\mu\text{m}$ of metal width.
- Mainly applies to $V_{\text{DD}}/V_{\text{SS}}$ lines.

Diffusion wire capacitance

- Capacitances formed by p-n junctions:
  - side-wall capacitances
  - depletion region
  - bottom-wall capacitance

Poly/metal wire capacitance

- Two components:
  - parallel plate;
  - fringe.
Metal coupling capacitances

- Can couple to adjacent wires on same layer, wires on above/below layers:

wire_layer_1

wire_layer_2

Wire resistance

- Resistance of any size square is constant:

Circuit simulation

- Circuit simulators like Spice numerically solve device models and Kirchoff’s laws to determine time-domain circuit behavior.

- Numerical solution allows more sophisticated models, non-functional (table-driven) models, etc.

Topics

- Fabrication defects and need for design rules
- Scalable design rules using unit λ
- Stick diagrams
- Standard-cell layout
Why we need design rules

- Masks are tooling for manufacturing.
- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Manufacturing problems

- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in temperature.
- Variations in oxide thickness.
- Impurities.
- Variations between lots.
- Variations across a wafer.

Transistor problems

- Variations in threshold voltage:
  - oxide thickness;
  - ion implantation;
  - poly variations.
- Changes in source/drain diffusion overlap.
- Variations in substrate.

Wiring problems

- Diffusion: changes in doping -> variations in resistance, capacitance.
- Poly, metal: variations in height, width -> variations in resistance, capacitance.
- Shorts and opens:
Oxide problems

- Variations in height.
- Lack of planarity -> step coverage.

Via problems

- Via may not be cut all the way through.
- Undersize via has too much resistance.
- Via may be too large and create short.

OK Too much resistance Disconnected

\( \lambda \) and design rules

- \( \lambda \) is the size of a minimum feature. However, the minimum wire width is usually \( 2\lambda \) (e.g. poly width = length of a transistor gate).
- Specifying \( \lambda \) particularizes the scalable rules.
- Parasitics are generally not specified in \( \lambda \) units.

Transistors
### Wires

- **metal 3**
- **metal 2**
- **metal 1**
- **pdiff/ndiff**
- **poly**

### Vias

- Types of via: metal1/diff, metal1/poly, metal1/metal2.

### Metal 3 via

- **Type**: metal3/metal2.
- **Rules**:
  - cut: 3 x 3
  - overlap by metal2: 1
  - minimum spacing: 3
  - minimum spacing to via1: 2

### Spacings

- **Diffusion/diffusion**: 3
- **Poly/poly**: 2
- **Poly/diffusion**: 1
- **Via/via**: 2
- **Metal1/metal1**: 3
- **Metal2/metal2**: 4
- **Metal3/metal3**: 4
Stick diagrams

- A stick diagram is a cartoon of a layout.
- Does show all components/vias (except possibly tub ties), relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick layers

- metal 3
- metal 2
- metal 1
- poly
- ndiff
- pdiff

Dynamic latch: full layout and stick diagram

Layout design and analysis tools

- Layout editors are interactive tools.
- Design rule checkers are generally batch: identify DRC errors on the layout.
- Circuit extractors extract the netlist from the layout.
- Connectivity verification systems (CVS) compare extracted and original netlists (also called LVS, layout versus schematics check).
The designer is given a library of elementary circuits called cells.

The design of library cells (from transistors) is a specialized task and is done by a dedicated group or company.

Library information consists of:
- cell function and simulation models (delays!)
- cell layouts.

Designing amounts to delivering a netlist of cells for layout.

The netlist is generally obtained by means of logic synthesis.

The netlist is mapped on a layout by means of placement and routing.

Cells use a limited number of metal layers.

Power wires run horizontally through the cells using the same pitch; horizontal cell abutment can be applied.

Other wires have terminals on the top and/or bottom of the cell; wiring channels realize the interconnection of terminals according to netlist.
Standard-cell layout (3)

- Cells are organized in multiple rows with wiring channels in between.
- Routing can use metal layers on top of cells.
- The aspect ratio (height vs. width) of a block of standard cells can be influenced.
- An entire chip will in general consist of multiple blocks of standard cells, as well as memories, data paths, etc.

Standard-cell layout (4)