**VLSI SYSTEM DESIGN (121713)**

- **RESPONSIBLE GROUP:**
  University of Twente, Department of Electrical Engineering
  Chair for Signals and Systems (EL-S&S)
- **INSTRUCTOR:** Dr. ir. SABIH H. GEREZ
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1) Also affiliated with National Semiconductor, Design Center Hengelo.

**GOALS**

- Familiarity with modern VLSI design techniques with an emphasis on *system-level* design issues.
- Knowledge of design flow and design automation tools used.
- Practical experience in VLSI design through small project.

**SHORT CONTENTS**

- Transistors and layout
- Logic gates
- Combinational logic
- Sequential logic, memories
- Subsystem design: adders, multipliers, etc.
- Floorplanning
- Architecture design
- Design automation
- Low-power design
- Case studies

**REQUIRED KNOWLEDGE**

- In principle, only knowledge from the compulsory part of the curriculum.
- For Electrical Engineering students, the ASC Design Laboratory (Practicum ASIC Design).
- For Computer Science students, Digital Techniques (Digitale Techniek), especially the last part on physical aspects.
- For the practical projects, knowledge of VHDL is assumed:
  – Refreshed in a separate lecture and introductory exercises.
  – In exceptional cases, alternative projects that don’t use VHDL are possible.
COURSE MATERIAL

- BOOK:
- Lecture slides. They contain material not covered in the book and are available through the course’s web page with URL: http://utelnt.el.utwente.nl/links/gerez/vlsisys/index.html.
- Possible other additional material. Will be announced during lectures and on the web page.

LECTURES

- About 10 lectures on Mondays 5th/6th hour;
- According to official schedule; beware of holidays and examination periods!

STUDY LOAD: 100 hours

- 10 lectures of 1.5 hours: 15 hours.
- Studying the book and other material: about 25 hours.
- Practical project: about 60 hours.

EXAMINATION (1)

- Practical project
- Preferably in teams of two students
- Start in second half of trimester; no deadline for termination.
- Many alternatives are possible depending on initiative of student
- For students without own ideas (most of them), there are standard projects (to be announced on web page)

EXAMINATION (2)

- In principle, projects are based on VHDL synthesis:
  - some introductory exercises to refresh knowledge of VHDL and its synthesizable subset;
  - a larger final project in which part of the theory presented in the course can be applied;
  - emphasis on design optimization (area, speed, power) rather than functional correctness only;
  - using modern industrial design tools (Modelsim for VHDL simulation and Synopsys for VHDL synthesis).
EXAMINATION (3)

- Final oral session (see also web page):
  - Maximal duration: 1 hour
  - Questions on report about project, exercises and rest of material
  - Team members take turn to answer
- *Project mark* based on report about final project, introductory exercises, and discussion during oral session (may not be the same for all team members).
- Performance on rest of material can lead to a *correction of project mark* by one point (up or down).

RELATED COURSES

- VLSI Signal Processing (122733)
- CAD Tools for VLSI (124153)
- Digital VLSI Circuit Design (121750)
- Testable Design and Testing of Integrated Microsystems (121716)
- Hardware/Software Co-Design (213012)